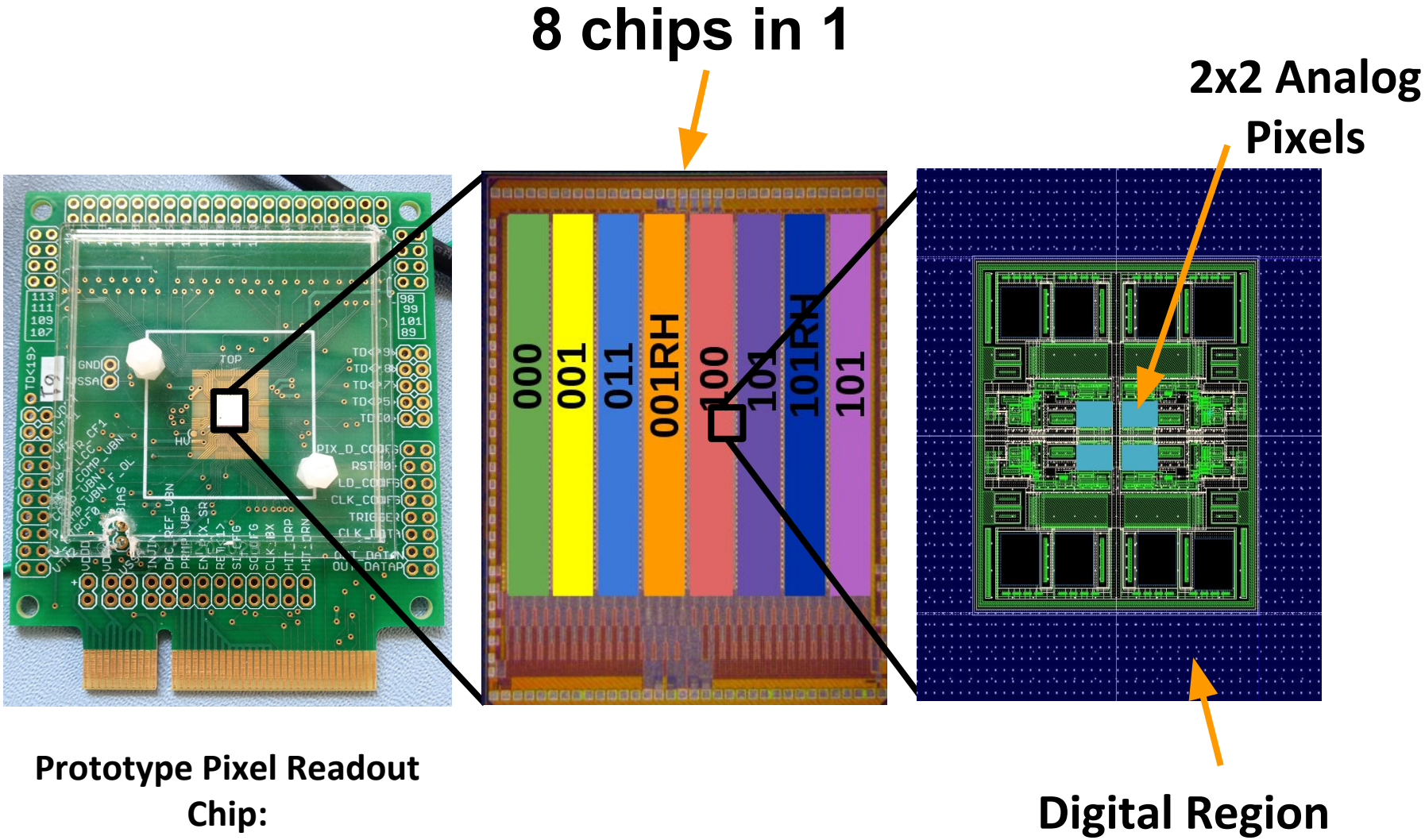
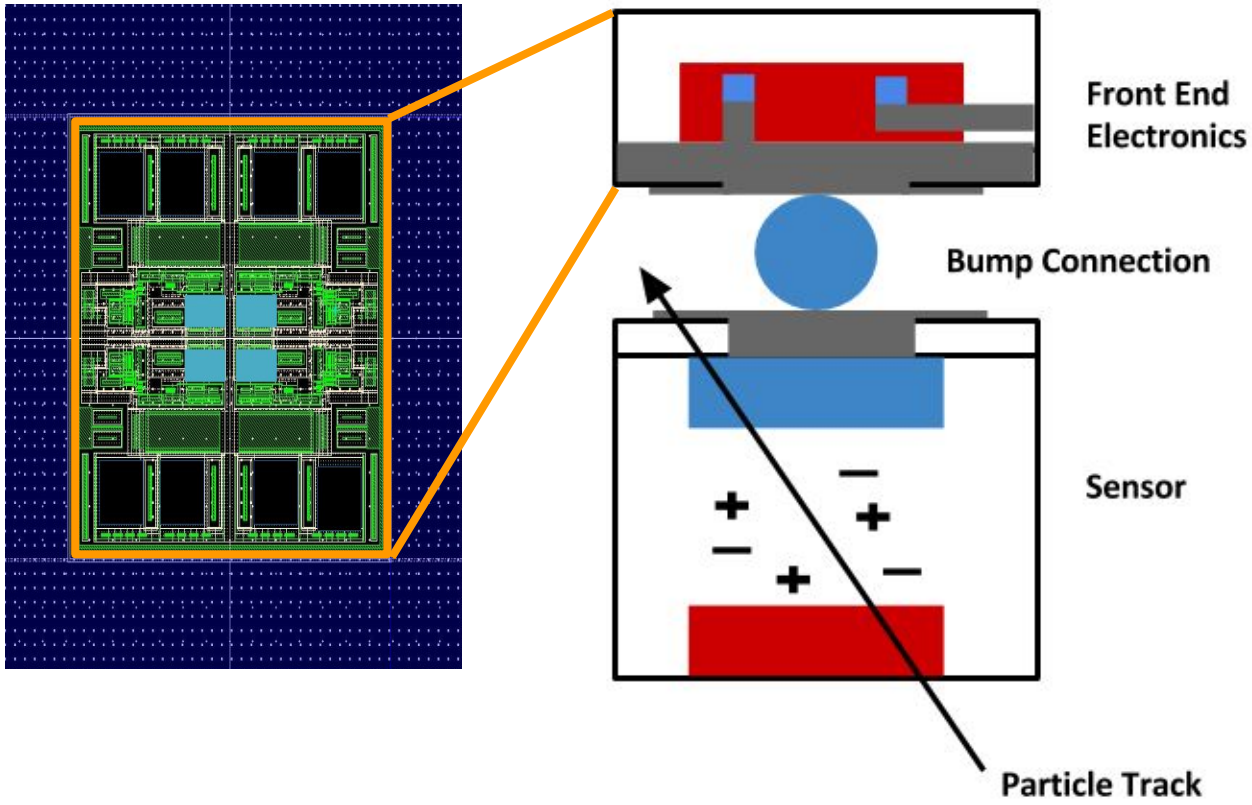
FE65-P2 Timing Dispersion

FE65-P2: Overview



Prototype Pixel Readout Chip:
Successor to FE-I4
Predecessor to RD53A

Hybrid Pixel Detectors

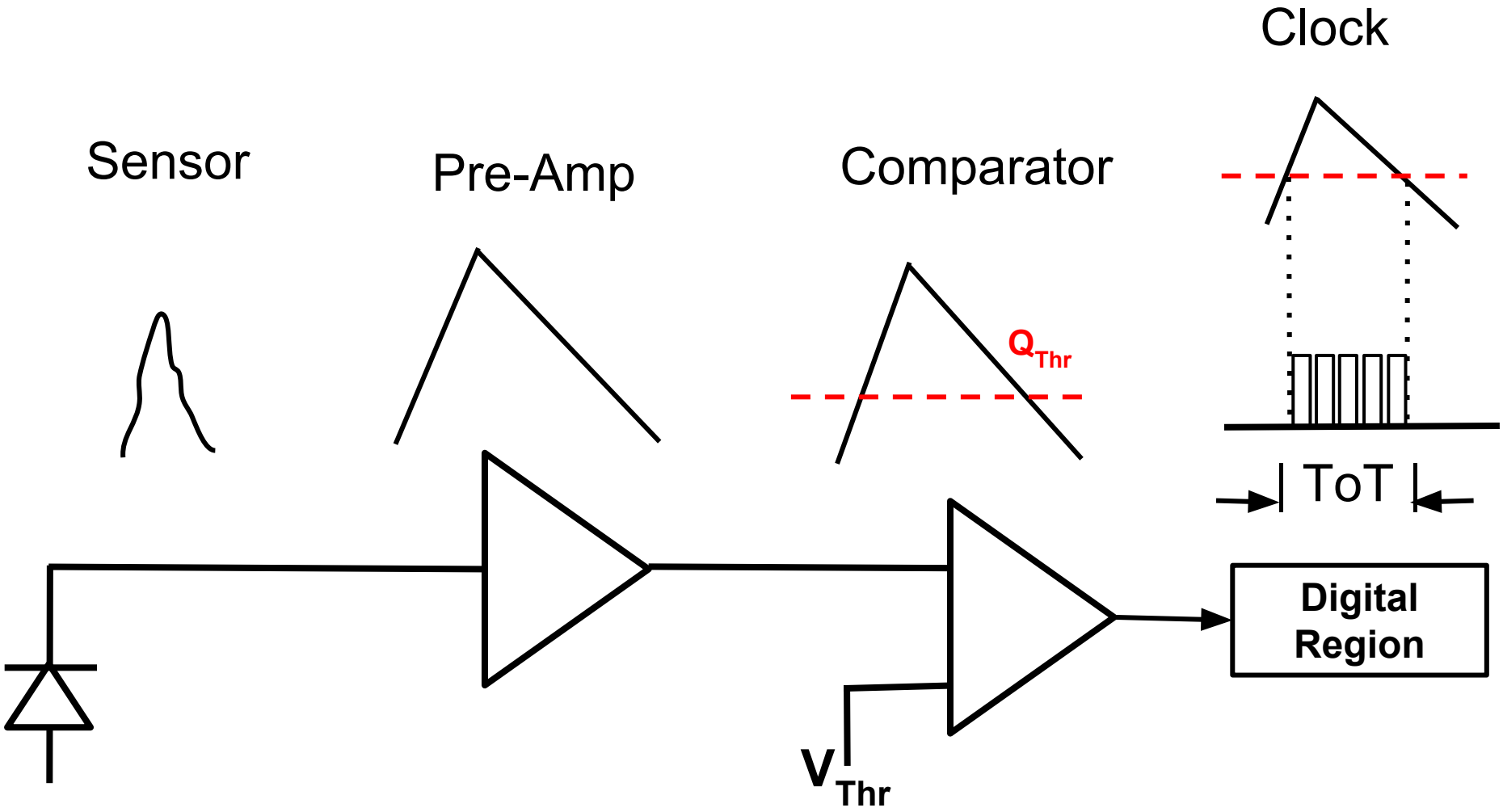


Sensor bump bonded to pads surrounding analog front ends

Charge is collected

FE65-P2: Overview

Tests done on chip without sensor: hit is simulated with injected charge

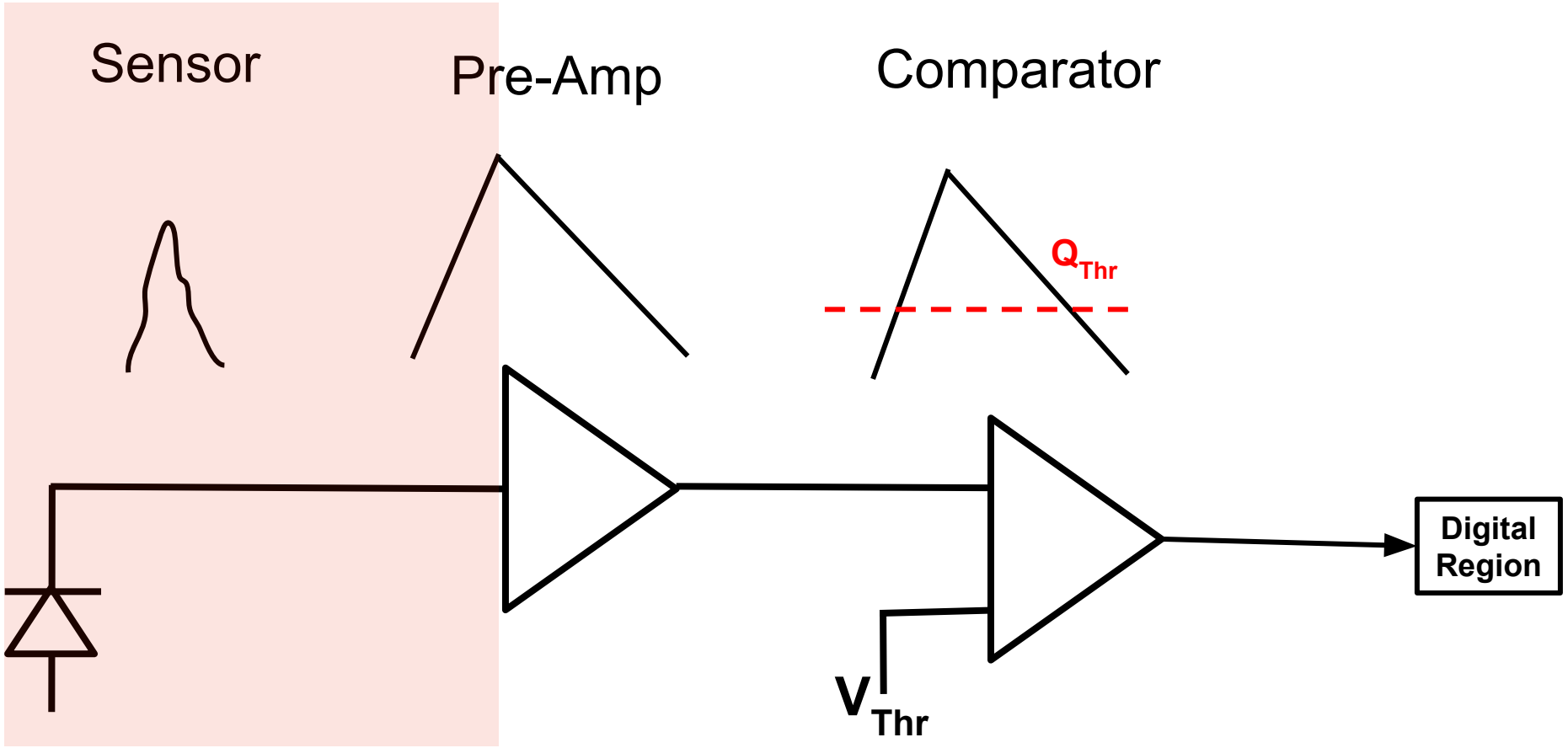


Propagation of Delay

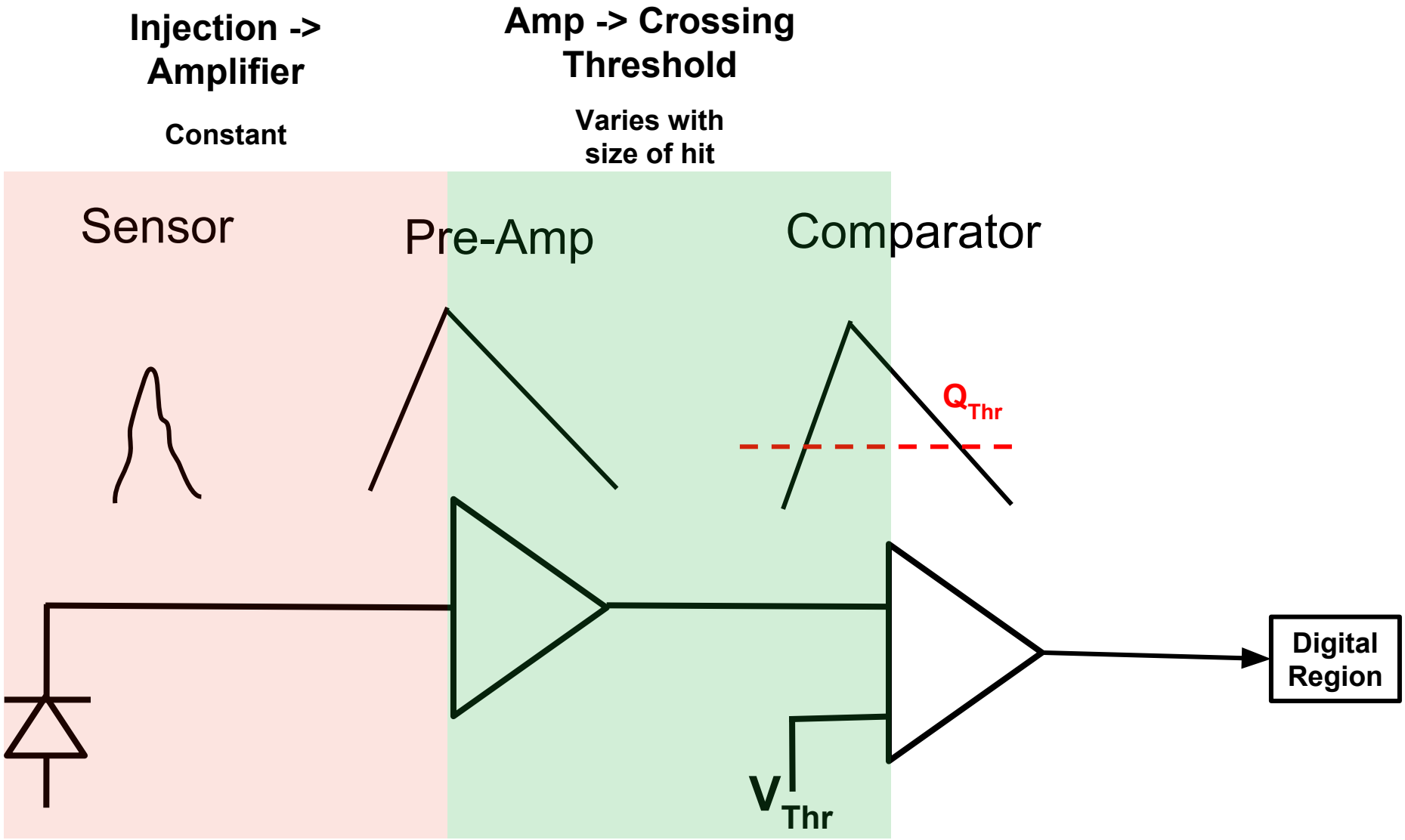
Delay

Injection -> Amplifier

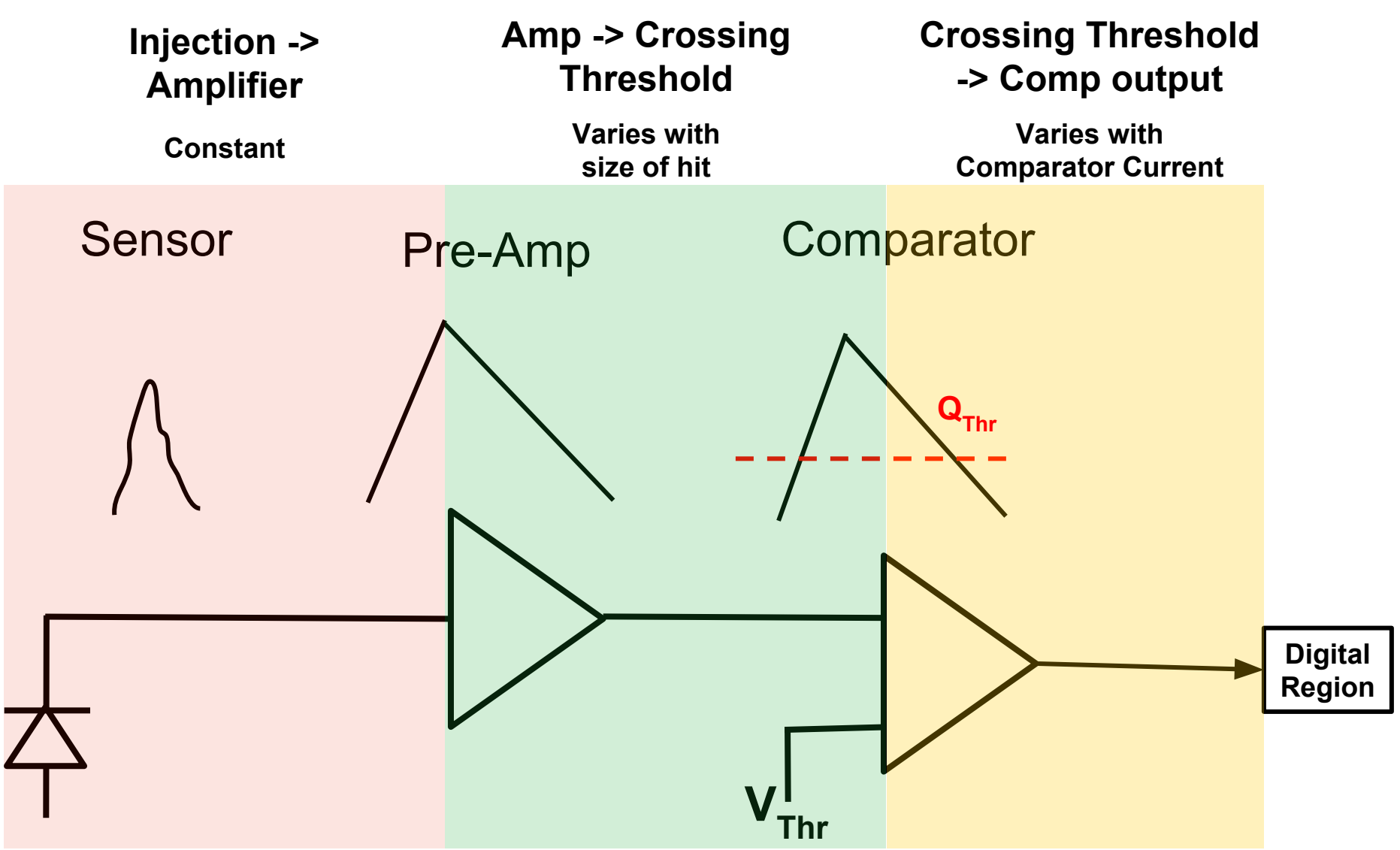
Constant



Delay


Injection -> Amplifier
Constant
Amp -> Crossing Threshold
Varies with size of hit
Sensor
Pre-Amp
Comparator
Q_{Thr}
V_{Thr}
Digital Region

Delay


Injection -> Amplifier
Constant
Amp -> Crossing Threshold
Varies with size of hit
Crossing Threshold -> Comp output
Varies with Comparator Current
Sensor
Pre-Amp
Comparator
Q_{Thr}
V_{Thr}
Digital Region

PlsrDelay Measurements

Per Pixel Delay

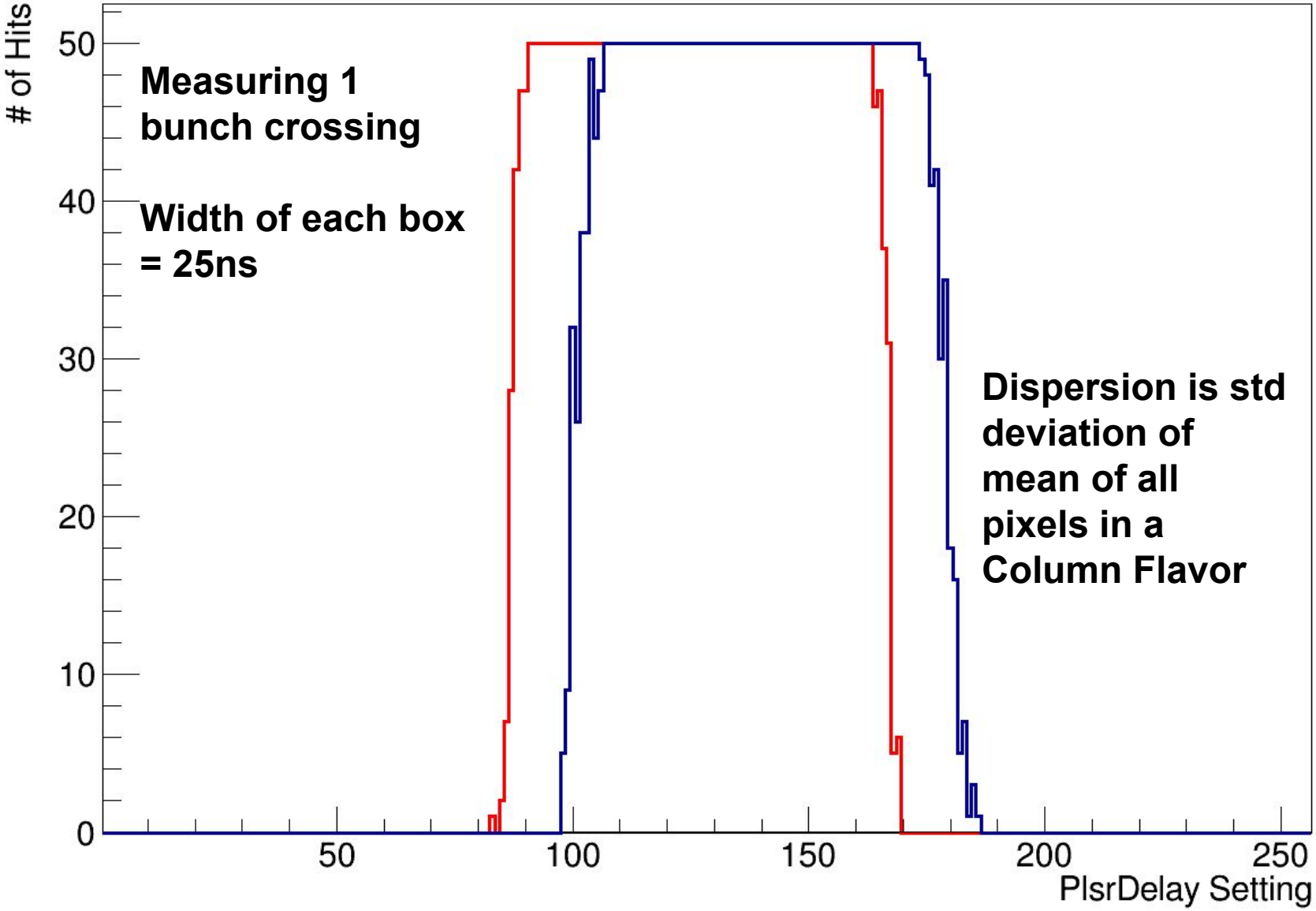
PlsrDelay is a 256 bit register with each bit corresponding to a specific delay in nanoseconds

Global Latency chosen so that sweeping through PlsrDelay settings 0->255 gives rising and falling edge in hit occupancy for each pixel

PlsrDelay scan is run at different Comparator currents
-> controlled by voltage bias: CompVbn

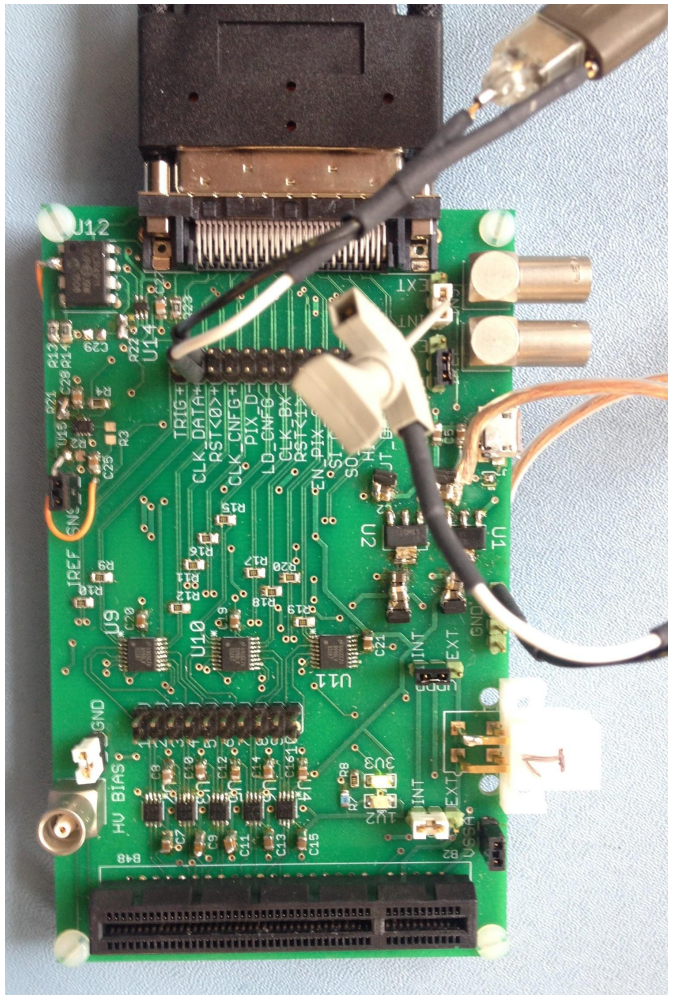
Mean delay in ns of each pixel is recorded

PlsDelay Measurements



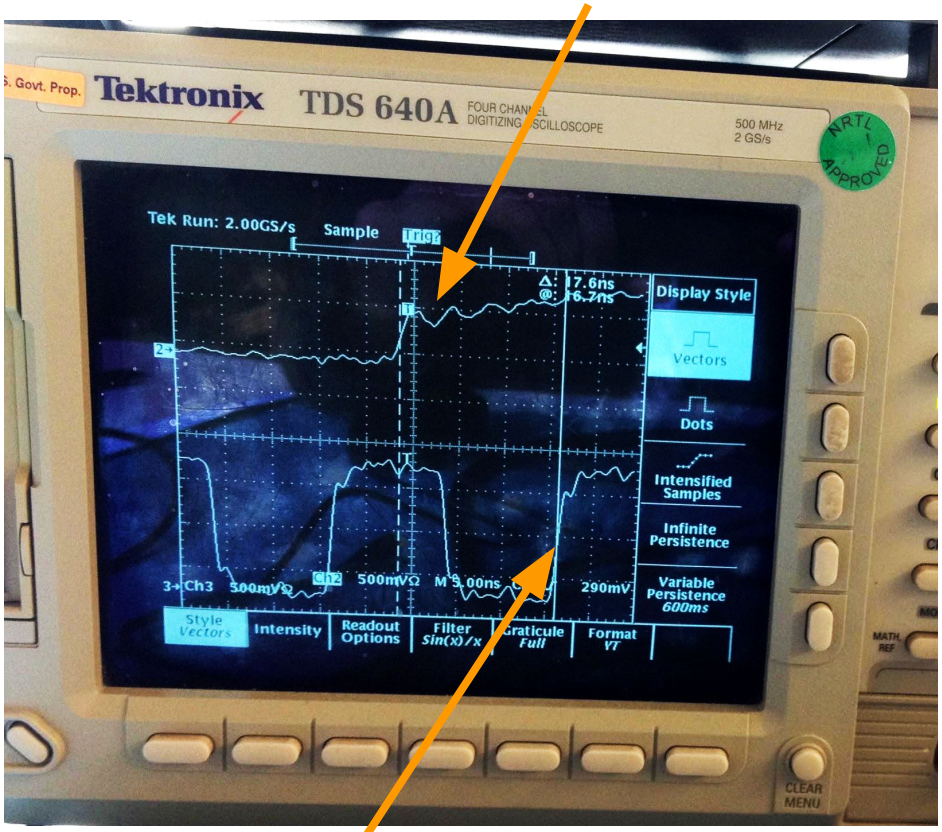
Setting -> Delay Conversion

Delay settings 0->255 must be converted to ns



PlsrDelay step size in nanoseconds is a property of test board

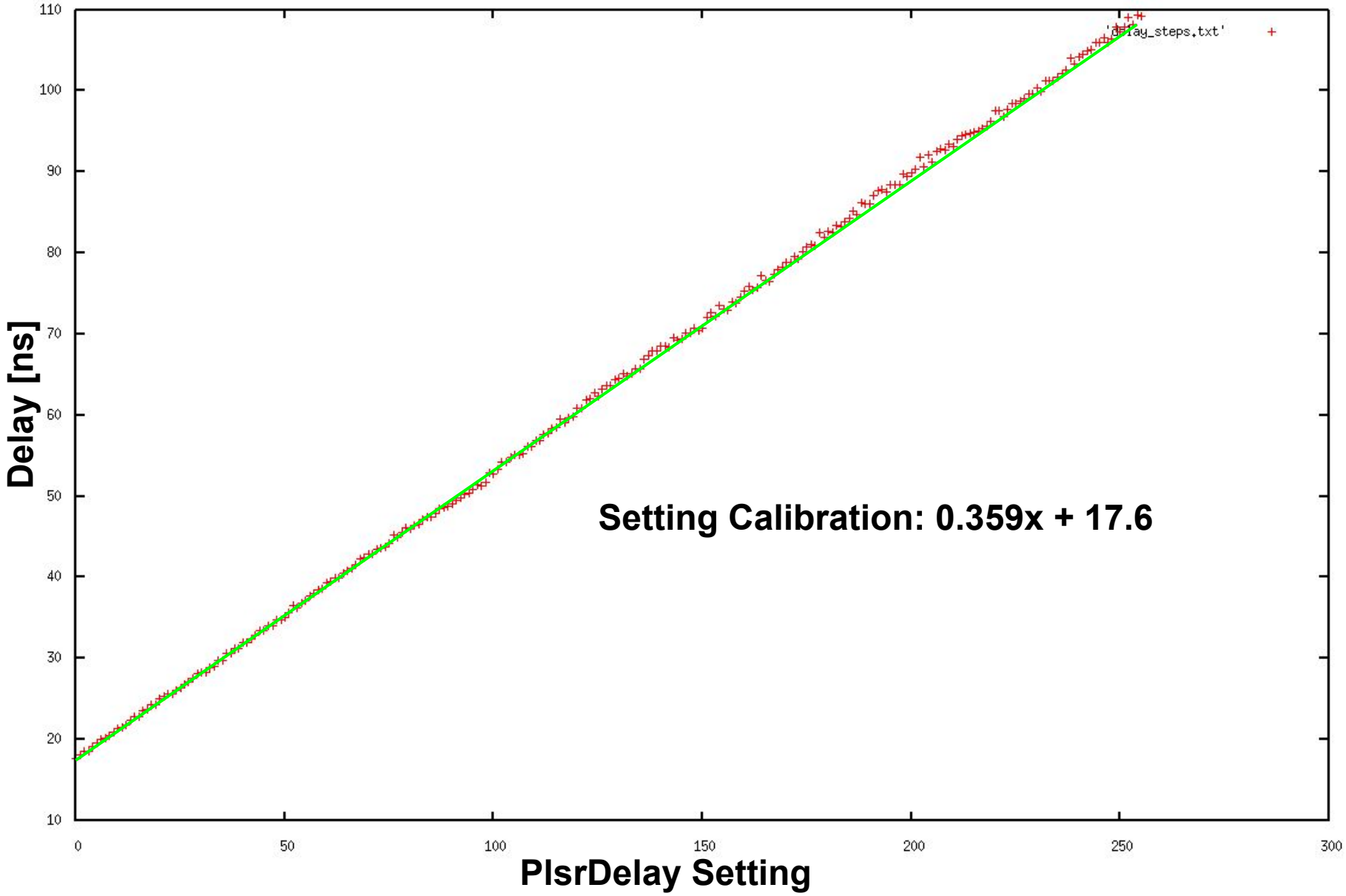
Injection



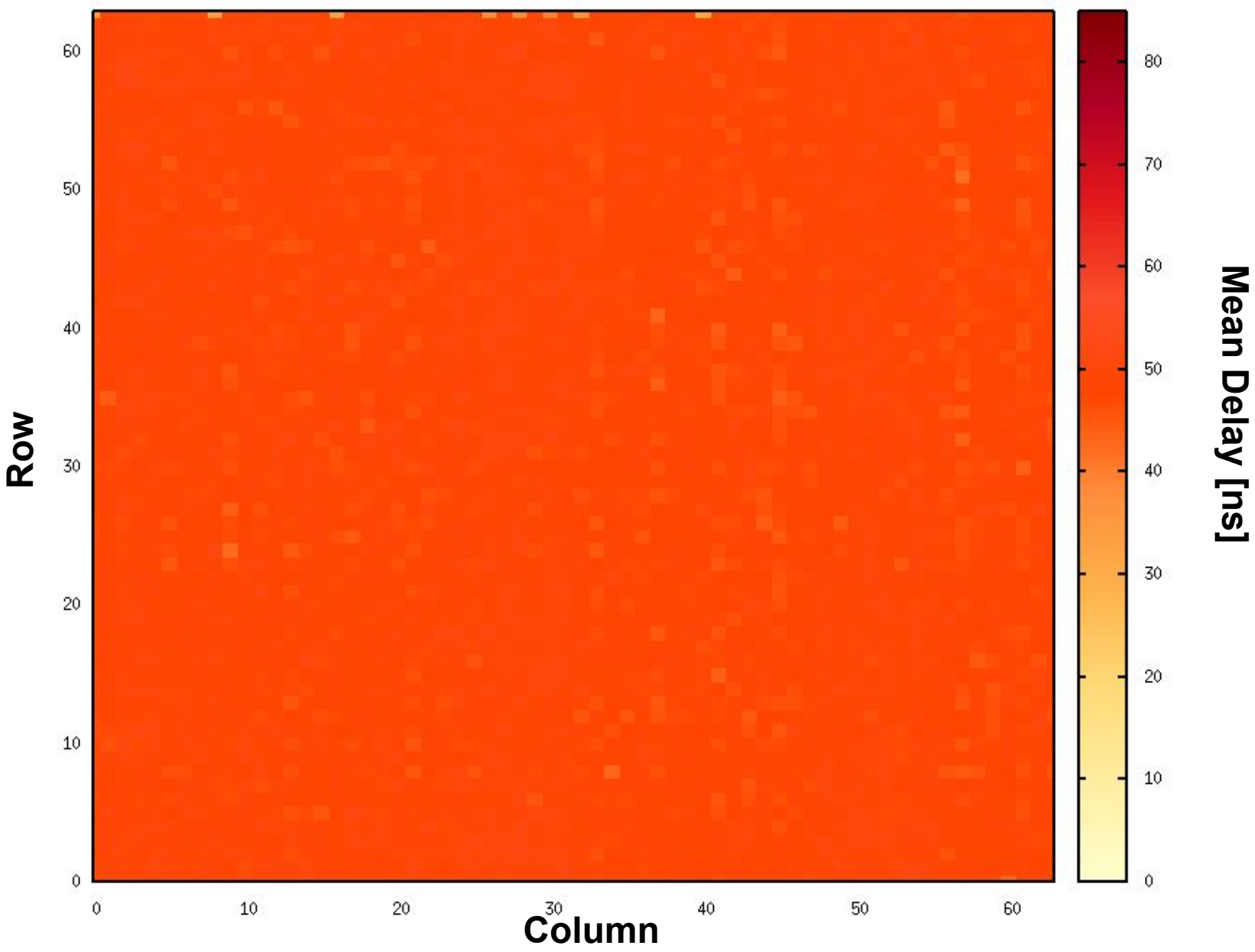
Clock

Measure Δt between clock & injection at each PlsrDelay setting

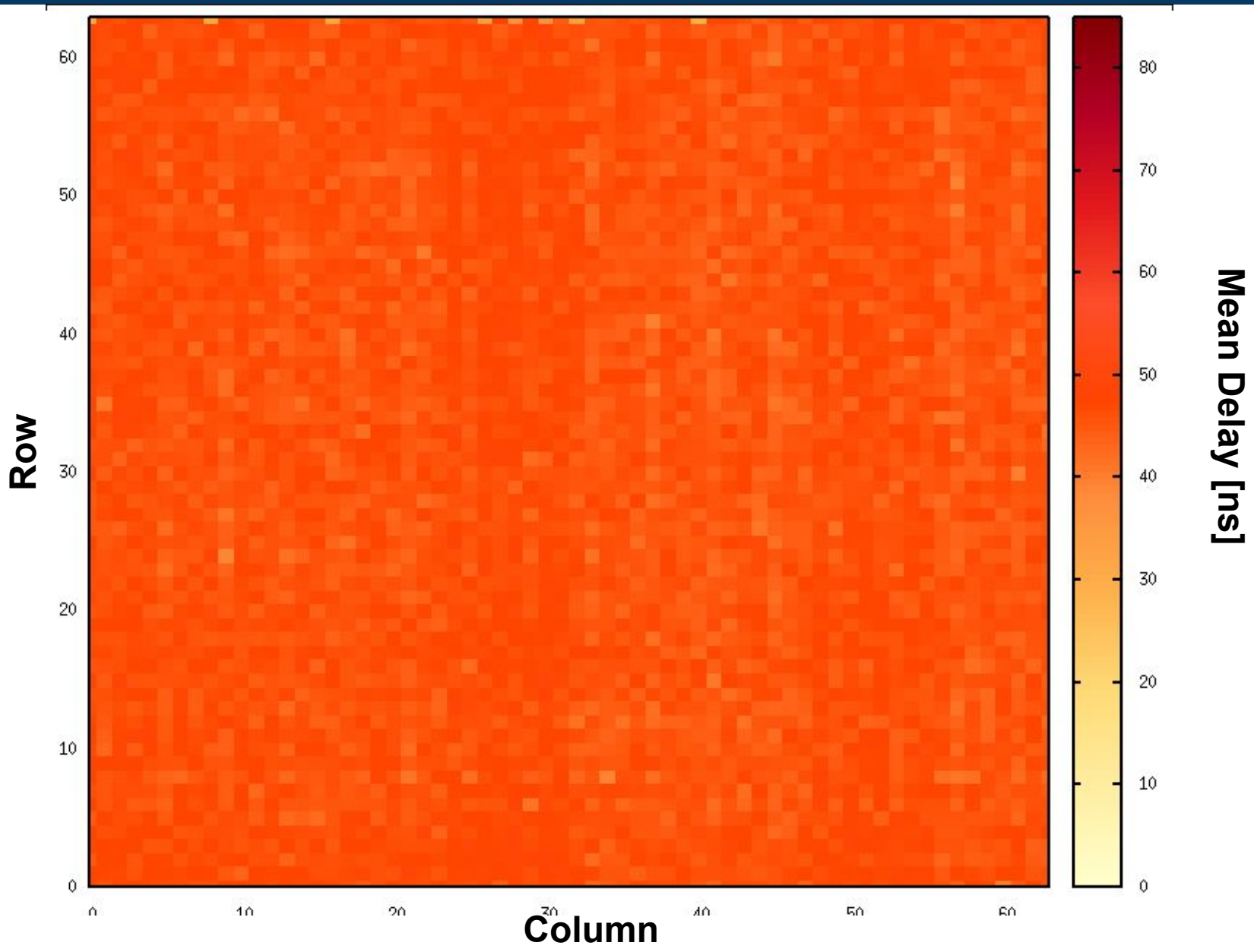
Setting -> Delay Conversion



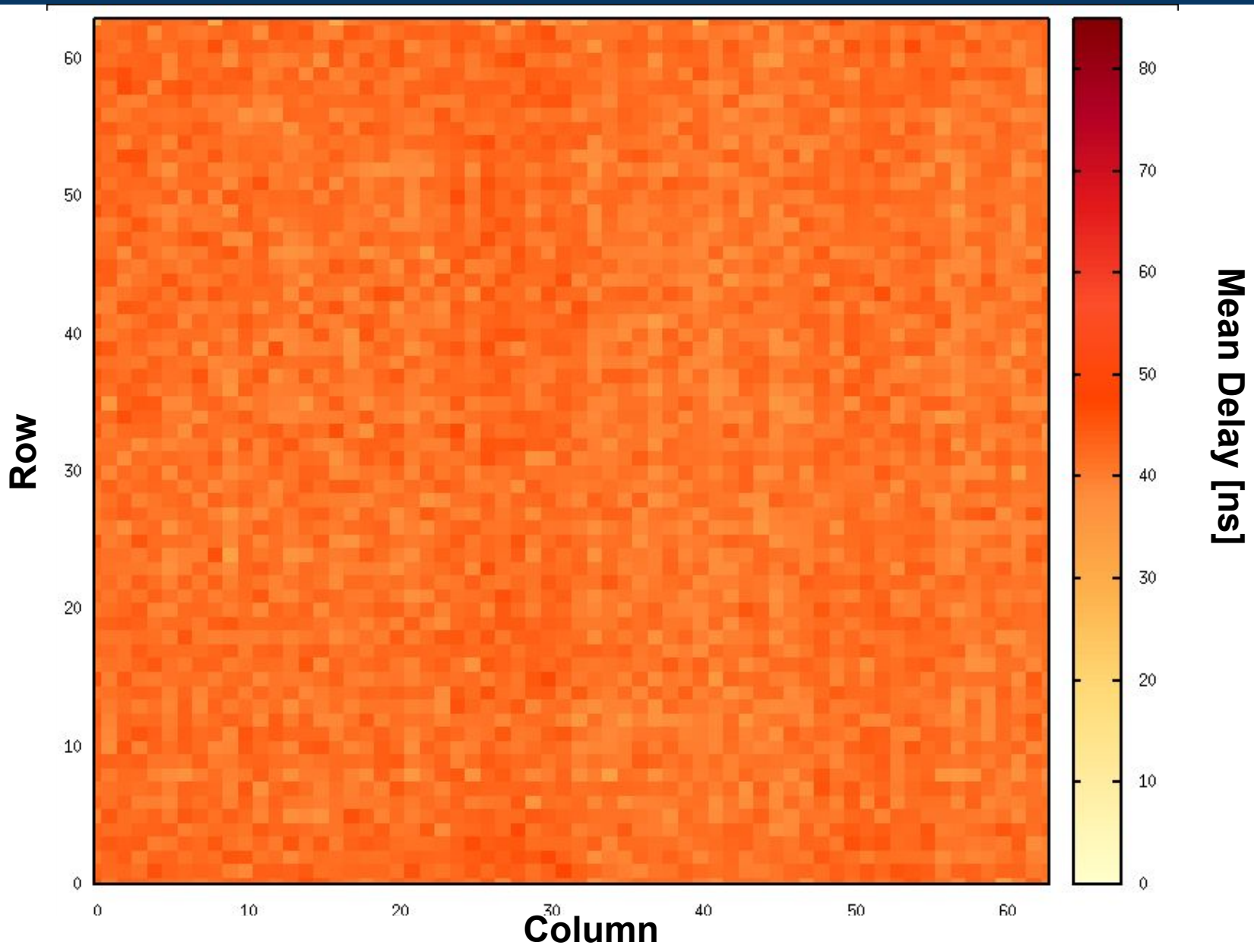
CompVbn: 60



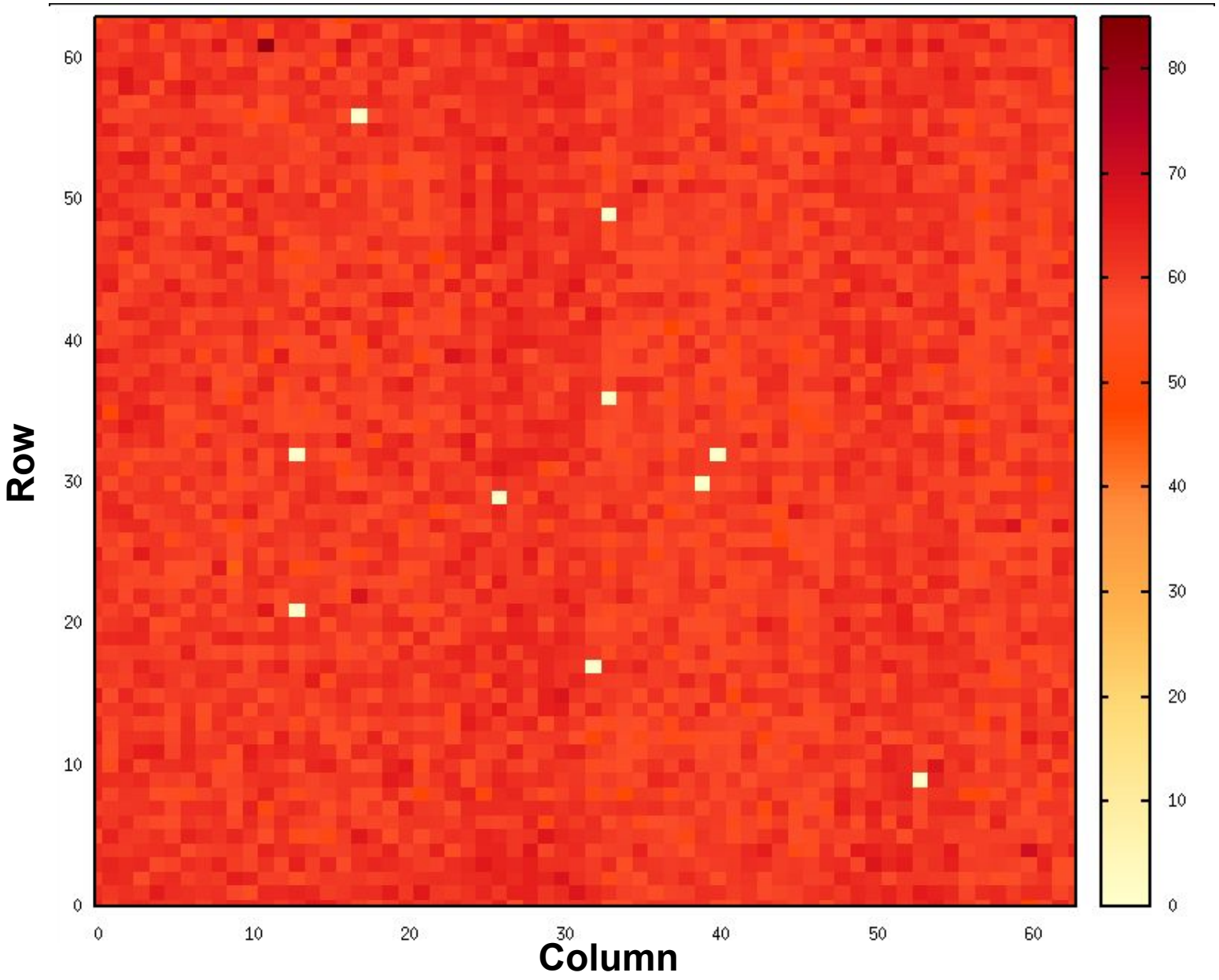
CompVbn: 50


Row
0
10
20
30
40
50
60
Column
0
10
20
30
40
50
60
Mean Delay [ns]
0
10
20
30
40
50
60
70
80

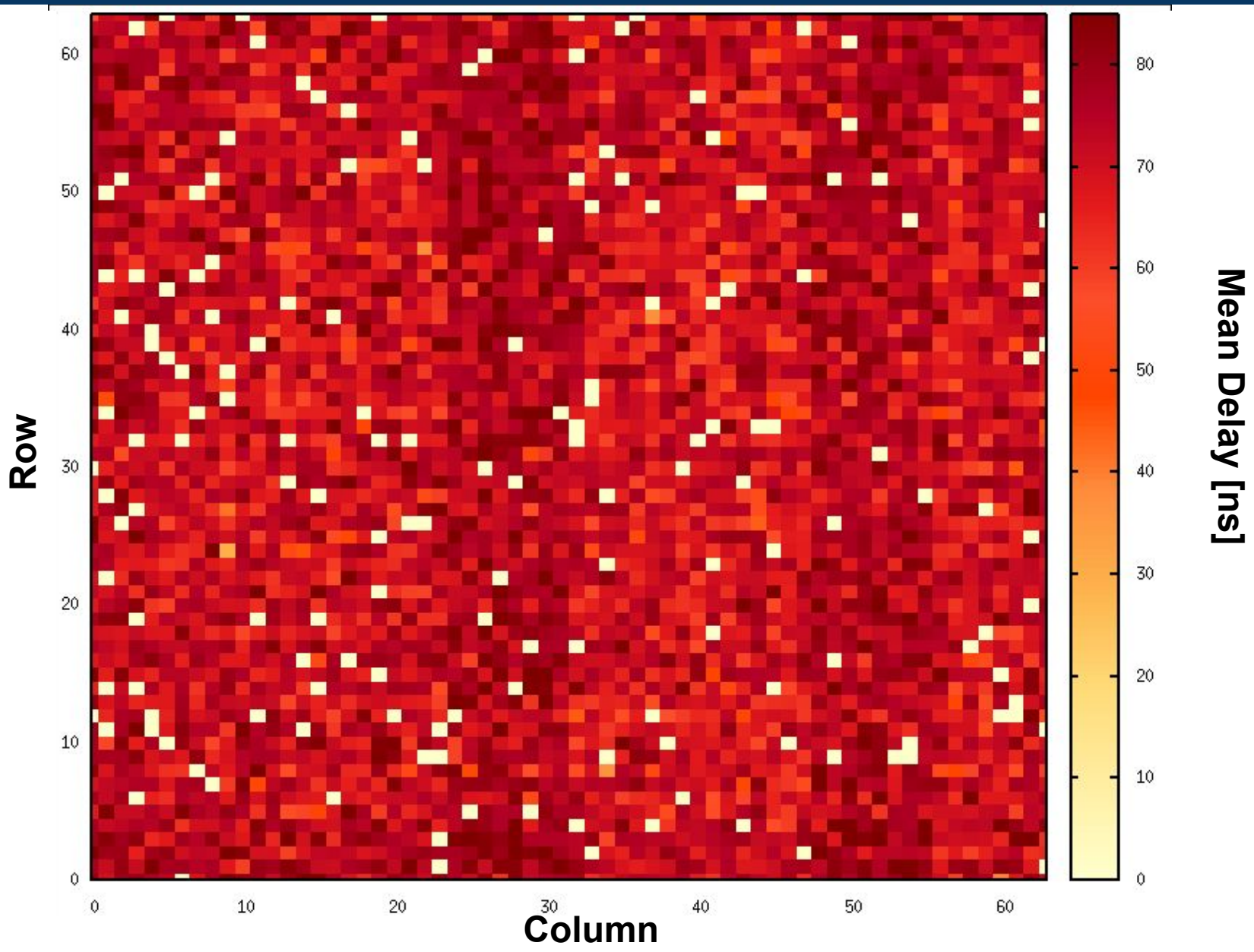
CompVbn: 40



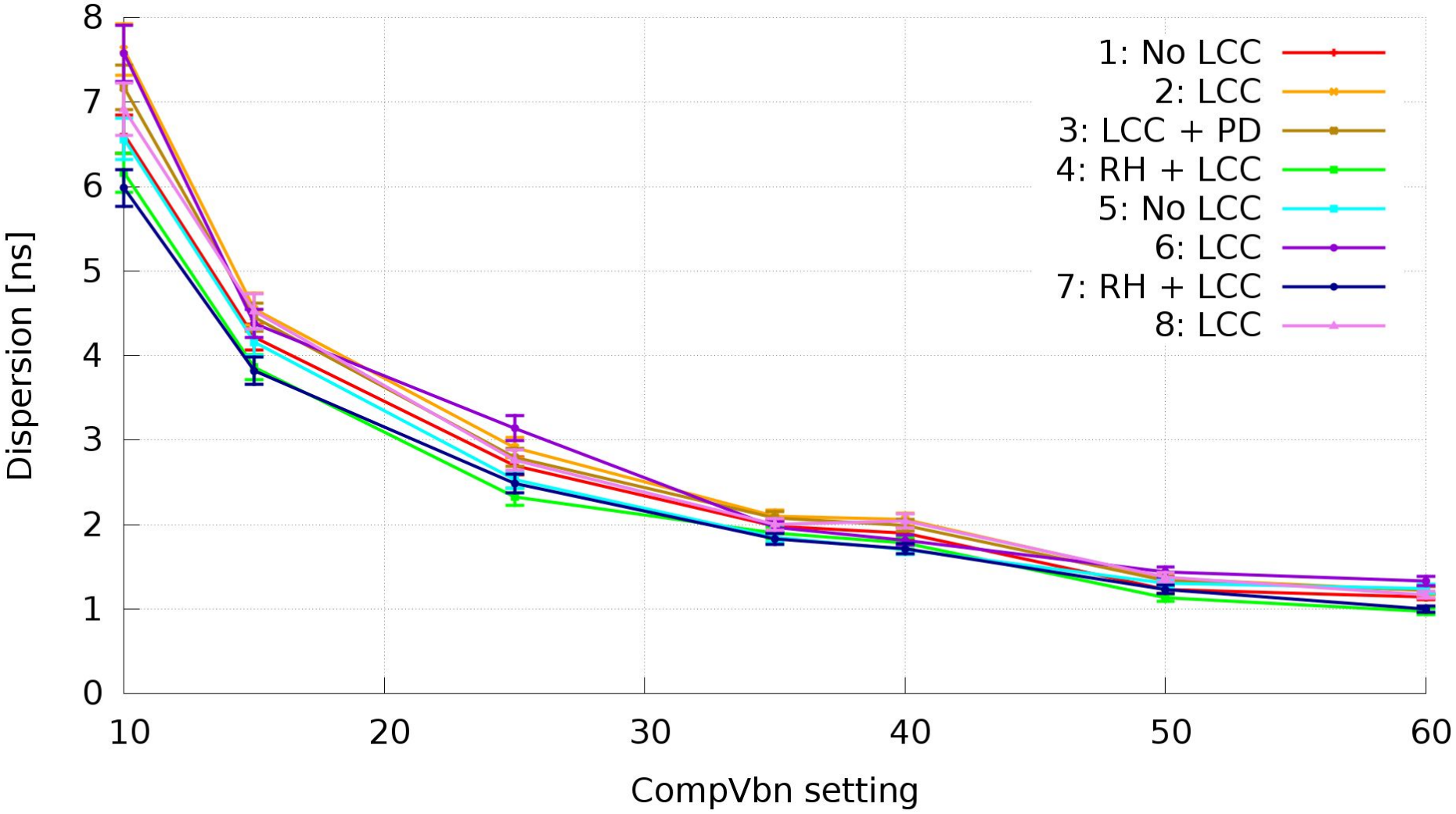
CompVbn: 25


Row
Column
Mean Delay [ns]
0
10
20
30
40
50
60
0
10
20
30
40
50
60
70
80

CompVbn: 10


Row
Column
Mean Delay [ns]
0
10
20
30
40
50
60
0
10
20
30
40
50
60
70
80

Column Flavor Dispersion

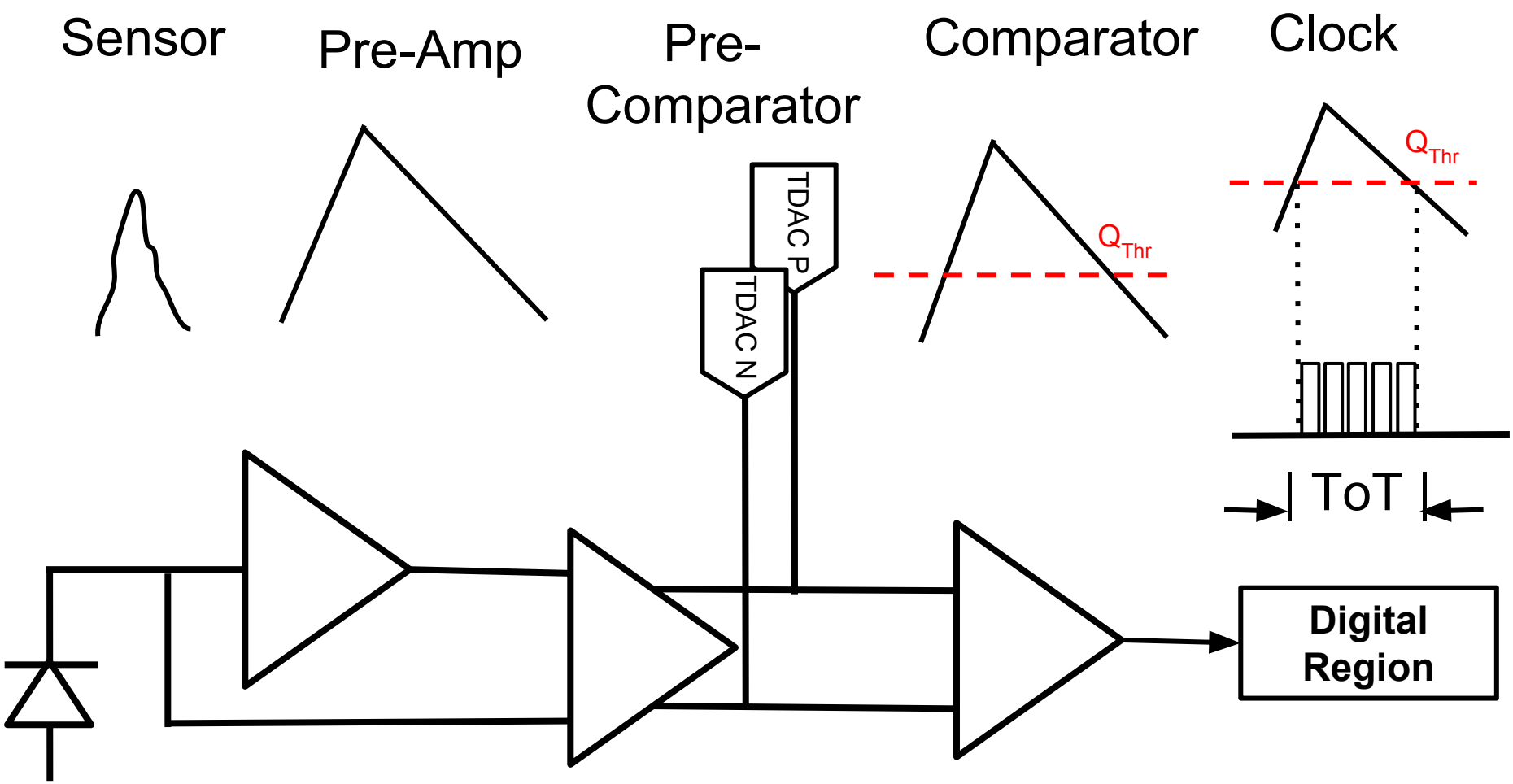


Next Steps

Compare how mean changes with Comparator current

-> have to make latencies comparable

PlsrDelay scans with different Pre-Amp current setting


Sensor
Pre-Amp
Pre-Comparator
Comparator
Clock
TDAC P
TDAC N
Q_{Thr}
Q_{Thr}
ToT
Digital Region